SALELF® 2S45 FPGA

Datasheet

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Content

1 Introduction

1.1 SALELF® 2S45 (hereafter refer to EF2S45) Features

- **Flexible Architecture**
  - 4,500 LUTs
  - Maximum user IOs up to 57
- **Low power**
  - Advanced low power consumption technology
  - Static power consumption lower to 5mA
  - Dual supply
- **Embedded FLASH**
  - Without external configuration devices
  - Fast power-on boot
- **Embedded and Distributed RAM**
  - Maximum support 35Kbits distributed RAM
  - Maximum support 700Kbits embedded RAM
  - 9k and 32k Block RAM that can be configured as true dual-port with multiple combination modes
  - ERAM9K has dedicated FIFO control logic
  - Support 128Kbits, 256Kbis large embedded RAM
- **Programmable Logic Blocks (PLBs)**
  - Optimized LUT4/LUT5 combinatorial design
  - Dual-port distributed memory
  - Arithmetic logic
  - Fast carry chain logic
- **Source Synchronous Input/ Output Interface**
  - Input/output units contain DDR register supporting DDRx1, DDRx2 modes.
- **High-performance, Flexible Input/ Output Buffer**
  - Following single-ended standards are available by configuration

    -LVTTL,

    LVCMOS(3.3/2.5/1.8/1.5/1.2V)

    - PCI
  - Following differential standards are available by configuration

    LVDS, LVPECL
  - Hot socketing
  - Programmable pull-up/pull-down mode
  - On-chip 100ohm differential resistor

- Optimized MIPI HS/LP IO Support

■ **Clock Resource**

- 16 Global Clock
- Two IOCLK for high-speed I/O interface each BANK
- Two fast clock for optimizing global clock
- Multi-functional PLLs for frequency synthesis
  - seven clock output
  - division factor from 1 to 128
  - Support five clock output cascading
  - Dynamic phase selection

■ **Configuration Mode**

- Master SPI (MSPI)
- JTAG Mode (IEEE-1532)

■ **BSCAN**

- Compatible with IEEE-1149.1

■ **Enhanced Security Design Protection**

- Unique 64-bit DNA for each Device

■ **Embedded Hard IP**

- Embedded ring oscillator

■ **Package Method**

- BGA

Table 1-1 EF2S45 Device Guide

Device	LUTs	DRAM (Kbs)	ERAM				Total (Kbits)	DSP	PLL	Flash	PSRAM	MAX user IO	MCU
			9K	32K	128K	256K							
EF2S45	4480	35	12	6	1	1	700	15	1	4Mb	64Mb	56	/
EF2M45	4480	35	12	6	1	1	700	15	1	4Mb	64Mb	56	1

Table 1-2 EF2S45 FPGA Package

Packages	EF2S45VG81	EF2M45VG81C
BGA (4.2x4.2, 0.4mm pitch)	56/ (15+8)	56/ (15+8)

Note 1: 56/(15+8) indicates: available user IO number/ (available user true differential pairs number+ pseudo differential pairs)

Note 2: BANK0/BANK2 only support 1.8V single-ended and differential voltage

1.2 Introduction to EF2S45

Built on the mature, reliable, programmable and low power consumption FPGA-EF2L45, EF2S45 FPGA integrate with two 4Mx8bits PSRAM using the advanced 3D packaging technology. It is ideally fit in applications that require large-scale, high-speed data sampling, transmission and conversion.

Special features:

- Multiple devices with large-scale embedded memory
  - Embed two 4Mx8bits PSRAMs with maximum working frequency of 200MHz and the maximum read/write bandwidth of 400MBps.
  - Embed 12 ERAM9K random read/write RAMs that can be configured as true dual-port, simple dual-port, single RAM and FIFO working mode, and the bit-width can be configured as 512x18, 1Kx9, 2Kx4, 4Kx2, 8Kx1 with the maximum frequency of 220Mhz.
  - Embed six ERAM32K random read/write RAMs that can be configured as single RAM, dual-port RAM being configured as 2Kx16 or 4Kx8.
  - Support 128Kbits, 256Kbits large-scale embedded memory.
- Smaller package allows more IOs that is beneficial for PCB routing and pin layout.
  - BGA81 package specification: 4.2x4.2mm, 0.4mm fine
  - Up to 56 user IOs
  - Embedded PSRAM do not occupy external user IO
  - Support True LVDS input/ output, the maximum receiving frequency of 800Mbps and maximum transmitting frequency of 800Mbps.
  - Embed 4Mbits SPI FLASH, after power-on, it can be opened to user.

2 EF2S45 Architecture

Same as EF2L45, for more information please refer *ELF2 FPGA Datasheet*.

3 EF2S45 AC/DC Characteristics

Same as EF2L45, for more details please refer to *ELF2 FPGA Datasheet*.

Note: BANK0/BANK2 only support 1.8B single-ended and differential voltage.

4 EF2S45 Embedded PSRAM

EF2S45 embeds two 4Mx8bits PSRAMs with maximum working frequency of 200Mhz and the maximum read/write bandwidth up to 400MB/s. PSRAM is deeply integrate with FPGA through the software. You can instantiate it in IP generate to implement PSRAM, or instantiate the following top module file. The IP porotype as shown in the following:

```
EF2_LOGIC_PSRAM u_ EF2_LOGIC_PSRAM (
                .SRAM_CE_N      ( SRAM_CE_N ),
                .SRAM_DQS       ( SRAM_DQS      ),
                .SRAM_DM        ( SRAM_DM       ),
                .SRAM_CLK_N     ( SRAM_CLK_N    ),
                .SRAM_CLK       ( SRAM_CLK      ),
                .SRAM_ADQ       ( SRAM_ADQ  )
)
```

Table 4-1 PSRAM IP Pin Distribution

PSRAM Pin	Direction	Width	Description
SRAM_CE_N	IN	1	Connect with PSRAM
SRAM_DQS	INOUT	1	Connect with PSRAM
SRAM_DM	IN	1	Connect with PSRAM
SRAM_CLK_N	IN	1	Connect with PSRAM
SRAM_CLK	IN	1	Connect with PSRAM
SRAM_ADQ	INOUT	8	Connect with PSRAM

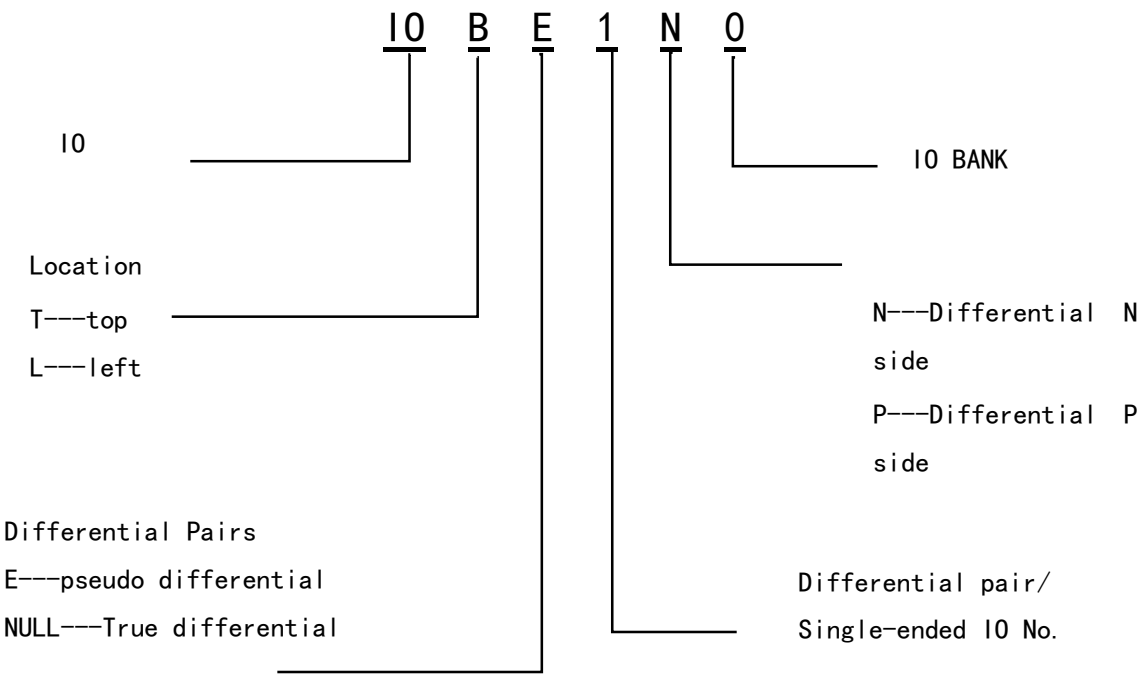
5 Pin and Package

5.1 Pin Definition

Table 5-1 Pin Naming Rule

Pin Name	Direction	Description
General I/O		
GND	—	Voltage Ground
VCC	—	Voltage supply for core (1.2V)
VCCIOx	—	Voltage supply for I/O BANK
VCCAUX	—	Auxiliary Voltage (2.5-3.3V)
JTAG Dedicated Pin		
TCK	Input	TCK input boundary scan clock
TDI	Input	Boundary scan data input
TDO	Output	Boundary scan data output
TMS	Input	Boundary scan mode select
JTAGEN	Input	JTAG access control pin
Configuration Dedicated Pin		
D[7:0]	Input	Configuration data input pin
SCLK	I/O	Configuration clock pin
Clock dedicated pin		
GCLKIO	Input	Global clock dedicated input pin

5.2 IO Naming Rule



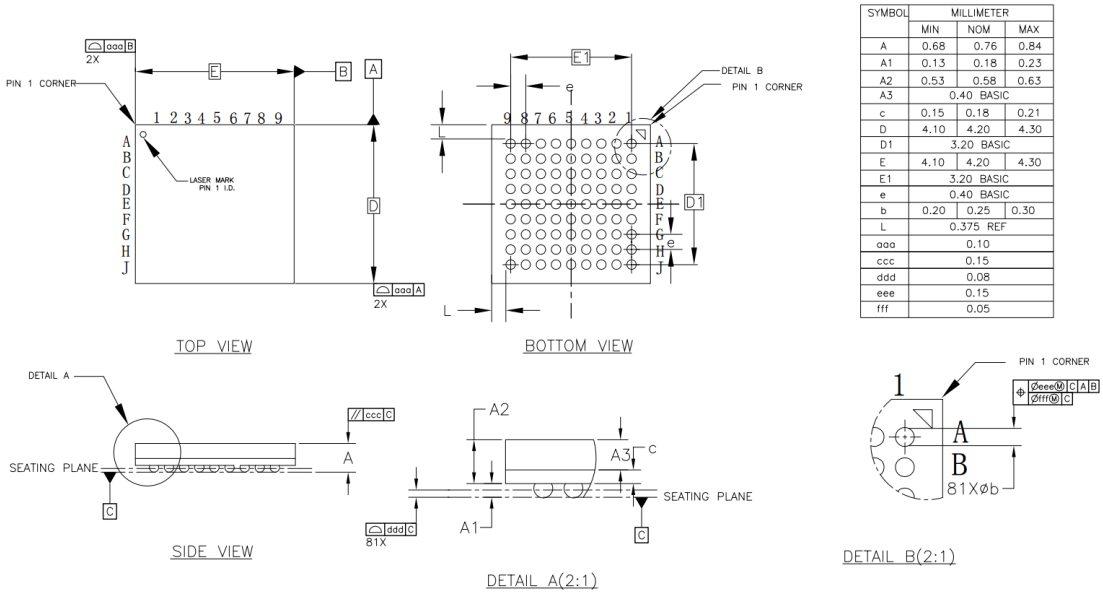
5.3 EF2S45VG81/EF2M45VG81C FPGA Pin List

No.	Type	BANK	Description	No.	Type	BANK	Description
B6	IOBB	0	IO_BE1P_0	A9	IOBE	1	IO_L7P_1
B7	IOBB	0	IO_BE1N_0	H2	IOBB	2	IO_TE1N_2
C5	IOBB	0	IO_B1_0	H3	IOBB	2	IO_TE1P_2
D4	IOBB	0	IO_BE2P_0, DO	J4	IOBB	2	IO_T1_2, DPCLKIO_7, ADC1_CH3
A7	IOBB	0	IO_BE2N_0, D1	H4	IOBB	2	IO_TE2N_2, GCLKIOT_3
B5	IOBB	0	IO_BE3P_0, D2	G4	IOBB	2	IO_TE2P_2, GCLKIOT_2
C4	IOBB	0	IO_BE3N_0, D3	H5	IOBB	2	IO_TE3N_2, ADC1_VREF
B4	IOBB	0	IO_BE4P_0, D4, GCLKIOB_4	H6	IOBB	2	IO_TE3P_2, ADC1_CH4
A4	IOBB	0	IO_BE4N_0, D5, GCLKIOB_5	G6	IOBB	2	IO_T2_2, ADC1_CH5
B3	IOBB	0	IO_BE5P_0, D6	H7	IOBB	2	IO_T3_2,
C3	IOBB	0	IO_BE5N_0, D7	J7	IOBB	2	IO_T4_2,
G7	IOBE	1	IO_L1P_1	H8	IOBB	2	IO_T5_2,
G8	IOBE	1	IO_L1N_1	A1	IOBE	3	IO_R1P_3
G5	IOBE	1	IO_L2N_1	B2	IOBE	3	IO_R1N_3
F5	IOBE	1	IO_L2P_1	D3	IOBE	3	IO_R2N_3
F8	IOBE	1	IO_L3P_1, ADC0_CH6	D2	IOBE	3	IO_R2P_3
F7	IOBE	1	IO_L3N_1, ADC0_CH7	C1	IOBE	3	IO_R3N_3
F6	IOBE	1	IO_L1_1, JTAGEN	D1	IOBE	3	IO_R3P_3
E9	IOBE	1	IO_L4P_1	E5	IOBE	3	IO_R4N_3
E8	IOBE	1	IO_L4N_1, DPCLKIO_1	D5	IOBE	3	IO_R4P_3
E7	IOBE	1	IO_L5N_1, ADC0_CH1, GCLKIOL_1	E3	IOBE	3	IO_R5N_3, GCLKIOR_1
E6	IOBE	1	IO_L5P_1, ADC0_CH2, GCLKIOL_0	E4	IOBE	3	IO_R5P_3, GCLKIOR_0
D7	IOBE	1	IO_L2_1, TMS	F1	IOBE	3	IO_R6P_3, SCLK
D8	IOBE	1	IO_L3_1, TCK	F2	IOBE	3	IO_R6N_3
C9	IOBE	1	IO_L4_1, TDO	F3	IOBE	3	IO_R7N_3, GPLL2_OUTN
C6	IOBE	1	IO_L5_1, TDI	F4	IOBE	3	IO_R7P_3, GPLL2_OUTP
C8	IOBE	1	IO_L6N_1	G1	IOBE	3	IO_R8P_3
C7	IOBE	1	IO_L6P_1	G2	IOBE	3	IO_R8N_3
B8	IOBE	1	IO_L7N_1				

No.	Type	BANK	Description		No.	Type	BANK	Description
J2	-	-	VCCAUX					
J9	-	-	VCCAUX					
C2	-	-	VCC					
B9	-	-	VCC					
J1	-	-	VCC					
H9	-	-	VCC					
A3	-	0	VCCIO0					
A6	-	0	VCCIO0					
A8	-	0	VCCIO0					
D6	-	1	VCCIO1					
G9	-	1	VCCIO1					
J3	-	2	VCCIO2					
J5	-	2	VCCIO2					
E1	-	3	VCCIO3					
B1	-	3	VCCIO3					
A2	-	-	GND					
A5	-	-	GND					
D9	-	-	GND					
E2	-	-	GND					
F9	-	-	GND					
G3	-	-	GND					
H1	-	-	GND					
J6	-	-	GND					
J8	-	-	GND					

Note: BANK0, BANK2 internally connected with PSRAM/FLASH voltage, only can connect to 1.8V.

5.4 EF2S45VG81/EF2M45VG81C Package Specification



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.68	0.76	0.84
A1	0.13	0.18	0.23
A2	0.53	0.58	0.63
A3		0.40 BASIC	
c	0.15	0.18	0.21
D	4.10	4.20	4.30
D1		3.20 BASIC	
E	4.10	4.20	4.30
E1		3.20 BASIC	
e		0.40 BASIC	
b	0.20	0.25	0.30
L		0.375 REF	
aaa		0.10	
ccc		0.15	
ddd		0.08	
eee		0.15	
fff		0.05	

6 Order Information

Table 6-1 Device Abbreviation

Device Name	Type	LUTs	Package	Temperature Grade
EF2	S	45	VG81	C

- Device Family
  - ✧ EF2: ELF2 Family Devices
- Type
  - ✧ S: SIP Device
- LUTs
  - ✧ 45: 4500 LUTs
- Package Method: <Type><#>
  - ✧ VG: Very Thin BGA
  - ✧ #: Pin number (81 refers to 81 pins)
- Temperature grade
  - ✧ C: Commercial (TJ = 0 - 85 ℃)
  - ✧ I: Industrial (TJ = -40 - 100 ℃)

Revision History

Date	Version	Change
2020/10/14	0.6	Update package information

Disclaimer